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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,320	01/08/2004	Robert C. Wong	END920030072US1 (16925)	7469

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,320	WONG, ROBERT C.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-23* is/are rejected.

7)☒ Claim(s) *8 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/08/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-24** are currently pending in the application is acknowledged.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 01/08/2004 and made of record. The references cited on the PTOL 1449 form have been considered.

Claim Objections

Claim **6** is objected to because of the following reasons.

Claim **6** should depend from claim **5** instead of claim **4**.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1-5, 7, 9, 11, 12, 14-17, 23 and 24** are rejected under 35 U.S.C. 102(b) as being anticipated by Hu et al. (USP 5,489,792 hereinafter referred to as "Hu").

Regarding claims **1-2, 4, 11, 12**, Hu discloses in Fig. 3 and the corresponding texts as set forth in column 4, lines 20-51, a selective silicon-on-insulator (SOI) structure comprises:

a silicon-on-insulator (SOI) substrate material 10, 12 comprising a top Si-containing layer (formed of P+ region 20, source region 16, drain region 14, and P doped body contact 18) having a plurality of SOI devices/MOSFETs having gate contact 24 located thereon, said SOI devices are in contact with an underlying Si-containing substrate (formed of buried silicon oxide layer 12 and Si substrate 10) via a body contact region (region under channel region 22); and

a DC node diffusion region/P+ region 20 adjacent to one of said SOI devices, said DC node diffusion region/the P+ region is in contact with said Si-containing substrate.

Regarding claim **3**, Hu discloses in Fig. 3 said plurality of SOI devices/MOSFETs are located atop a top Si-containing layer of said SOI substrate material.

Regarding claim **5**, Hu discloses in Fig. 3 said active source/drain regions are located atop a buried oxide 12.

Regarding claims **7 and 23**, Hu discloses in Fig. 3 said DC node diffusion region/the P+ region comprises a region in which a source voltage can be applied, a region in which a reference voltage can be applied, a ground region or any combination.

Regarding claim **9**, Hu discloses in Fig. 3 the MOSFETS comprise a gate dielectric (not labeled) and a gate conductor 24.

Regarding claim **14**, Hu discloses in Fig. 3 and the corresponding texts as set forth in column 4, lines 20-51, an integrated circuit comprising at least one selective silicon-on-insulator (SOI) structure said at least one selective SOI structure comprises a silicon-

on-insulator (SOI) substrate material 10, 12 comprising a top Si-containing layer (formed of P+ region 20, source region 16, drain region 14, and P doped body contact 18) having a plurality of SOI devices/MOSFETs having gate contact 24 located thereon, said SOI devices are in contact with an underlying Si-containing substrate (formed of buried silicon oxide layer 12 and Si substrate 10) via a body contact region (region under channel region 22); and a DC node diffusion region/P+ region 20 adjacent to one of said SOI devices, said DC node diffusion region is in contact with said Si-containing substrate.

Regarding claim **15**, Hu discloses in Fig. 3 and the corresponding texts as set forth in column 4, lines 20-51, a semiconductor substrate comprises:

an SOI substrate 10, 12;

a DC node diffusion region/P+ region 20 in said SOI substrate; and

a buried oxide material 12 within said SOI substrate, wherein said DC node diffusion region is in contact with an underlying Si-containing substrate (formed of buried silicon oxide layer 12 and Si substrate 10) of said SOI substrate.

Regarding claims **16 and 17**, Hu discloses in Fig. 3 said SOI substrate includes a top Si-containing layer (formed of P+ region 20, source region 16, drain region 14, and P doped body contact 18), wherein the top Si-containing layer and the underlying Si-containing substrate (formed of buried silicon oxide layer 12 and Si substrate 10) are composed of a silicon semiconductor material selected from the group consisting of Si, SiGe, SiC, SiGeC, Si/si, Si/SiC, and Si/SiGeC.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **6 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (USP 5,489,792 hereinafter referred to as "Hu") in view of Figs. 1A-1B, Applicant's admitted prior art (AAPA).

Regarding claim **6**, Hu discloses the above claimed limitations except for the buried oxide is a lateral etched area located adjacent to a trench isolation region. Figs. 1A-1B of AAPA teach that the buried oxide 14 is a lateral etched area located adjacent to a trench isolation region 12. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the buried oxide is a lateral etched area located adjacent to a trench isolation region to form a body contact as taught by Figs. 1A-1B of AAPA.

Regarding claim **22**, Hu discloses the above claimed limitations except for the semiconductor substrate further comprises at least one trench isolation region that is in contact with said buried oxide material. Figs. 1A-1B of AAPA teach that the semiconductor substrate comprises at least one trench isolation region 12 that is in contact with said buried oxide material 14. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form at least one trench

isolation region that is in contact with said buried oxide material for device or active region isolation.

Claim **10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (USP 5,489,792 hereinafter referred to as "Hu") in view of Kono et al. (JP 359119723A hereinafter referred to as "Kono").

Hu discloses the above claimed limitations except for the SOI substrate is an additive SOI substrate having discriminative regions for forming said DC node diffusion region. Kono discloses in Fig. 1 a discriminating region 14 for discriminating an impurity region formed in a semiconductor substrate 11 to avoid a breaking at a stepped part of a wiring and the like as set forth in English Abstract. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a discriminating region for discriminating an impurity region formed in a semiconductor substrate, as taught by Kono in order to avoid a breaking at a stepped part of a wiring and the like.

Claims **13 and 18-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (USP 5,489,792 hereinafter referred to as "Hu").

Regarding claims **13, 18 and 21**, Hu discloses the above claimed limitations except for the top Si-containing layer has a thickness from about 50 to about 200 nm, and the buried oxide material has a thickness from about 30 to about 100 nm. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the top Si-containing layer has a thickness from about 50 to about 200 nm, and the

buried oxide material has a thickness from about 30 to about 100 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim **19 and 20**, Hu discloses the above claimed limitations except for wherein the buried oxide material is crystalline or non-crystalline. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the buried oxide material is crystalline or non-crystalline, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Allowable Subject Matter

Claims **8 and 24** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hu, Kono and 1A-1B of AAPA, taken alone or in combination, fail to teach the claimed invention the selective SOI structure wherein said DC node diffusion region is located within bulk Si without oxide underneath.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

01/11/05

Andy Huynh

Patent Examiner